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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,336	10/01/2003	Hong-Ki Kim	8836-199 (IB12118-US)	6515

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,336	KIM ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/01/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 8 is objected to because of the following informalities: The word "sacrificial" in line 2 should be changed to "supporting." See page 9, paragraph 2 of the specification. Appropriate correction is required.

Claim 10 is objected to because of the following informalities: The word "and" in the third line should be changed to "or." See page 5, first full paragraph and page 7, first full paragraph of the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Won et al. (U.S. 6,653,186).

With respect to claim 1, Won et al. teaches a method of forming a capacitor by sequentially forming a supporting layer (**105** in Figure 6; column 3, lines 53-56) comprising a lower mold layer (**106** in Figure 6) and etch stop (**108** in Figure 6), and an upper mold layer (**110** in Figure 6) on a semiconductor substrate (**100** in Figure 6). The upper mold layer is later removed by a wet etch process (column 6, lines 17-18), so the upper mold layer is sacrificial. Won et al. teaches that the sacrificial upper mold layer and the supporting lower mold layer and etch stop are patterned to form an opening

(**111** in Figure 7; column 5, lines10-15). Won et al. teaches forming a bottom electrode (**114** in Figure 9) that covers the inner wall and bottom of the opening (Figure 9; column 6, lines 50-53). Won et al. teaches removing the sacrificial upper mold layer by a wet etch process (column 6, lines 17-18). Won et al. teaches forming a dielectric layer and an upper electrode on the bottom electrode and the supporting layer (Figure 5; column 6, lines 38-44). Since Won et al. teaches that the supporting layer comprises an etch-stop layer used to stop the wet etch of the sacrificial layer, the sacrificial layer has a faster wet etch rate than the supporting layer.

With respect to claim 2, Won et al. teaches forming a bottom contact plug (**104** in Figure 6) on the semiconductor substrate (**100** in Figure 6) before forming the supporting layer (column 4, lines 56-59; Figure 6), wherein the opening exposes the bottom contact plug and the opening has a wider width than the bottom contact plug (Figure 7).

With respect to claim 7, Won et al. teaches a method of forming a capacitor by sequentially forming a supporting layer (**105** in Figure 6; column 3, lines 53-56) comprising a lower mold layer (**106** in Figure 6) and etch stop (**108** in Figure 6), and an upper mold layer (**110** in Figure 6) on a semiconductor substrate (**100** in Figure 6). The upper mold layer is later removed by a wet etch process (column 6, lines 17-18), so the upper mold layer is sacrificial. Won et al. teaches that the sacrificial upper mold layer and the supporting lower mold layer and etch stop are patterned to form an opening (**111** in Figure 7; column 5, lines10-15). Won et al. teaches removing the sacrificial upper mold layer by a wet etch process (column 6, lines 17-18). Since Won et al.

teaches that the supporting layer comprises an etch-stop layer used to stop the wet etch of the sacrificial layer, the sacrificial layer has a faster wet etch rate than the supporting layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 5, 9, 10, 11 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Won et al. (U.S. 6,653,186) in view of Yu et al. (U.S. 6,624,018) and Fernandes et al. (U.S. 5,310,626).

With respect to claims 3 and 4, Won et al. teaches the method as claimed in claim 1 (note 35 U.S.C. 102(b) rejection above). Won et al. does not expressly teach that the supporting layer is formed of a plasma-enhanced tetraethyl orthosilicate (PETEOS) oxide or a high-density plasma (HDP) oxide, or that the sacrificial layer is formed of one material selected from a group consisting of a hydrogen silsesquioxane (HSQ) oxide, a borophosphosilicate glass (BPSG) oxide and a phosphosilicate (PSG) oxide.

Yu et al. teaches a method of fabricating a DRAM device through a process that includes forming a stack of insulator layers comprising layers of HDP silicon oxide (**12**a-e in Fig. 3; column 4, lines 6-8, 16-19, 21-24) and borophosphosilicate glass (BPSG) (**13**a-c in Fig. 3; column 4, lines 3, 16, 21). Yu et al. expressly teaches that the mode of

deposition for the silicon oxide layers, as well as the weight percents of the BPSG layers will be critical for selective wet etching characteristics, to subsequently be employed to define a specific capacitor opening shape (column 4, lines 28-32). Yu et al. also expressly teaches that an HF vapor procedure is used to selectively form lateral recesses in BPSG layers (**13**a-c in Fig. 3), while HDP silicon oxide layers (**12**a-e in Fig. 3) remain unetched (column 5, lines 7-10).

Fernandes et al. teaches a method for forming a semiconductor device wherein a wet HF etch can be used interchangeably with an HF vapor phase etch to etch an oxide (column 4, lines 55-56).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the invention as disclosed by Won et al. by stacking layers of HDP oxide and BPSG oxide, as taught by Yu et al., to act as the supporting layer and sacrificial layer, respectively.

The motivation for doing so at the time of invention would have been to take advantage of their selective etch characteristics in the presence of an HF vapor phase etch, as expressly taught by Yu et al. (column 5, lines 7-10), or an equivalent HF wet etch, as taught by Fernandes et al. (column 4, lines 55-56).

With respect to claim 5, Won et al. teaches the method as claimed in claim 1 (note 35 U.S.C. 102(b) rejection above). Won et al. does not expressly teach that the wet etch process is performed using an HF solution.

Yu et al. teaches a method of selectively etching BPSG oxide more quickly than HDP oxide (column 5, lines 7-10). Fernandes et al. teaches a method for forming a

semiconductor device wherein a wet HF etch can be used interchangeably with an HF vapor phase etch to etch an oxide (column 4, lines 55-56).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of fabricating a capacitor as taught by Won et al. and claim 1 by using an HF solution to perform the wet etch process, as disclosed by the combined teachings of Yu et al. and Fernandes et al.

The motivation for doing so at the time of invention would be because HF is known to etch BPSG more quickly than it etches HDP oxide, as expressly taught by Yu et al. (column 5, lines 7-10).

With respect to claims 9 and 10, Won et al. teaches the method as claimed in claim 7 (note 35 U.S.C. 102(b) rejection above). Won et al. does not expressly teach that the supporting layer includes a plasma-enhanced tetraethyl orthosilicate (PETEOS) oxide or a high-density plasma (HDP) oxide, or that the sacrificial layer includes a hydrogen silsesquioxane (HSQ) oxide, a borophosphosilicate glass (BPSG) oxide and a phosphosilicate (PSG) oxide.

Yu et al. teaches a method of fabricating a DRAM device through a process that includes forming a stack of insulator layers comprising layers of HDP silicon oxide (**12**a-e in Fig. 3; column 4, lines 6-8, 16-19, 21-24) and borophosphosilicate glass (BPSG) (**13**a-c in Fig. 3; column 4, lines 3, 16, 21). Yu et al. expressly teaches that the mode of deposition for the silicon oxide layers, as well as the weight percents of the BPSG layers will be critical for selective wet etching characteristics, to subsequently be employed to define a specific capacitor opening shape (column 4, lines 28-32). Yu et al.

also expressly teaches that an HF vapor procedure is used to selectively form lateral recesses in BPSG layers (**13**a-c in Fig. 3), while HDP silicon oxide layers (**12**a-e in Fig. 3) remain unetched (column 5, lines 7-10).

Fernandes et al. teaches a method for forming a semiconductor device wherein a wet HF etch can be used interchangeably with an HF vapor phase etch to etch an oxide (column 4, lines 55-56).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the invention as disclosed by Won et al. by stacking layers of HDP oxide and BPSG oxide, as taught by Yu et al., to act as the supporting layer and sacrificial layer, respectively.

The motivation for doing so at the time of invention would have been to take advantage of their selective etch characteristics in the presence of an HF vapor phase etch, as expressly taught by Yu et al. (column 5, lines 7-10), or an equivalent HF wet etch, as taught by Fernandes et al. (column 4, lines 55-56).

With respect to claim 11, Won et al. teaches the method as claimed in claim 7 (note 35 U.S.C. 102(b) rejection above). Won et al. does not expressly teach that the wet etch process is performed using an HF solution.

Yu et al. teaches a method of selectively etching BPSG oxide more quickly than HDP oxide (column 5, lines 7-10). Fernandes et al. teaches a method for forming a semiconductor device wherein a wet HF etch can be used interchangeably with an HF vapor phase etch to etch an oxide (column 4, lines 55-56).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of fabricating a capacitor as taught by Won et al. and claim 7 by using an HF solution to perform the wet etch process, as disclosed by the combined teachings of Yu et al. and Fernandes et al.

The motivation for doing so at the time of invention would be because HF is known to etch BPSG more quickly than it etches HDP oxide, as expressly taught by Yu et al. (column 5, lines 7-10).

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Won et al. in view of Saito et al (U.S. 6,399,438).

With respect to claim 6, Won et al. teaches the method of claim 1 (note 35 U.S.C. 102(b) rejection above). Won et al. does not expressly teach forming a dielectric layer over an entire surface of the semiconductor substrate comprising the upper electrode; patterning the dielectric layer to form a contact hole; and filling the contact hole with a conductive material to form a contact plug.

Saito et al. teaches a method of forming a semiconductor device comprising forming a dielectric layer (**63** in Fig. 3) over an entire surface of the semiconductor substrate (**1** in Fig. 3) comprising an upper electrode (**47** in Fig. 3); patterning the dielectric layer to form a contact hole (column 13, lines 53-54; **60** in Fig. 3); and filling the contact hole with a conductive material to form a contact plug (column 13, lines 58-60; **62** in Fig. 3).

Therefore, at the time of invention it would have been obvious to a person of ordinary skill in the art to modify the teaching of Won et al. by adding a dielectric layer

over the entire surface of the semiconductor substrate comprising the upper electrode; patterning the dielectric layer to form a contact hole; and filling the contact hole with a conductive material to form a contact plug, as taught by Saito et al.

The motivation for doing so at the time of invention would have been to incorporate the capacitor into a three-dimensional, stacked capacitor structure to compensate for a decrease in the charge storage quantity per information storing capacitive element, as taught by Saito et al. (column 1, lines 34-36, 50-51).

With respect to claim 8, Won et al. teaches the method of claim 7 (note 35 U.S.C. 102(b) rejection above). Won et al. does not expressly teach forming a dielectric layer over a supporting layer; patterning the dielectric layer and the supporting layer; and filling the contact hole with a conductive material to form a contact plug.

Saito et al. teaches a method of forming a semiconductor device comprising forming a dielectric layer (**63** in Fig. 3) over a supporting layer (**56** in Fig. 3); patterning the dielectric layer and the supporting layer to form a contact hole (column 13, lines 53-54; **60** in Fig. 3); and filling the contact hole with a conductive material to form a contact plug (column 13, lines 58-60; **62** in Fig. 3).

Therefore, at the time of invention it would have been obvious to a person of ordinary skill in the art to modify the teaching of Won et al. by adding a dielectric layer over a supporting layer; patterning the dielectric layer and the supporting layer to form a contact hole; and filling the contact hole with a conductive material to form a contact plug, as taught by Saito et al.

The motivation for doing so at the time of invention would have been to incorporate the capacitor into a three-dimensional, stacked capacitor structure to compensate for a decrease in the charge storage quantity per information storing capacitive element, as taught by Saito et al. (column 1, lines 34-36, 50-51).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kim et al. (Pub. No. US 2003/0032238) and Kim et al. (U.S. 6,500,763) describe methods of forming capacitors from semiconductor substrates using support and sacrificial layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty whose telephone number is (571) 272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

had

ERIK KIELIN
PRIMARY EXAMINER